REMARKS

The present Amendment amends claims 1,9, 10, 13, 16, 25 and 26, leaves claims 2, 4-6, 11, 14, 15, 17, 19-22 and 28-31 unchanged, and cancels claims 3, 7, 8, 12, 18, 23, 24, 27, 32 and 33. Therefore, the present application has pending claims 1, 2, 4-6, 9-11, 13-17, 19-22, 25, 26 and 28-31.

Claims 1-3, 9, 10, 12, 15-18 and 25-27 stand rejected under 35 USC §103(a) as being unpatentable over Myers (U.S. Patent Application Publication No. 2003/0071799) in view of Murata (U.S. Patent No. 6,009,305); claims 4, 19 and 28 stand rejected under 35 USC §103(a) as being unpatentable over Myers, in view of Murata and further in view of Monroe (U.S. Patent No. 7,131,136 B2); claims 5, 13, 14, 20, 21, 29 and 30 stand rejected under 35 USC §103(a) as being unpatentable over Myers, in view of Murata and further in view of Ueno (U.S. Patent No. 5,479,206); claims 6, 22 and 31 stand rejected under 35 USC §103(a) as being unpatentable over Myers, Murata in view of Ueno and further in view of Monroe; and claim 11 stands rejected under 35 USC §103(a) as being unpatentable over Myers, Murata and further in view of Tonkin (U.S. Patent No. 6,084,631). As indicated above claims 3, 7, 8, 12, 18, 23, 24, 27, 32 and 33 were canceled. Therefore, these rejections with respect to claims 3, 7, 8, 12, 18, 23, 24, 27, 32 and 33 are rendered moot. Accordingly, reconsideration and withdrawal of these rejections with respect to claims 3, 7, 8, 12, 18, 23, 24, 27, 32 and 33 is respectfully requested.

It should be noted that the cancellation of claims 3, 7, 8, 12, 18, 23, 24, 27, 32 and 33 was not intended nor should it be considered as an agreement

on Applicants part that the features recited in claims 3, 7, 8, 12, 18, 23, 24, 27, 32 and 33 are taught or suggested by any of the references of record whether taken individually or in combination with each other. The cancellation of claims 3, 7, 8, 12, 18, 23, 24, 27, 32 and 33 was simply intended to expedite prosecution of the present application. Applicants hereby reserve their right to pursue the subject matter as set forth in claims 3, 7, 8, 12, 18, 23, 24, 27, 32 and 33 in a continuing application.

These rejections are traversed with respect to the remaining claims 1, 2, 4-6, 9-11, 13-17, 19-22, 25, 26 and 28-31 for the following reasons. Applicants submit that the features of the present invention as now recited in claims 1, 2, 4-6, 9-11, 13-17, 19-22, 25, 26 and 28-31 are not taught or suggested by Myers, Murata, Monroe, Ueno or Tonkin whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to the claims to more clearly describe features of the present invention as recited in the claims. Particularly, amendments were made to the claims to recite that the present invention is directed to a apparatus for signal transmission between a television camera and a video apparatus, a method for signal transmission between a television camera and a video apparatus which are connected to each other through a transmission cable, a television camera apparatus for transmitting signals to a video apparatus, and a method for transmission from the television camera apparatus to the video apparatus.

According to the present invention the apparatus for signal transmission between a television camera and a video apparatus includes a first connection circuit which is connected to the television camera, a second connection circuit which is connected to the video apparatus, and a transmission cable for electrically connecting the first connection circuit and the second connection circuit to each other.

Further, according to the present invention the first connection circuit includes a first time-division multiplexing circuit for time division multiplexing an image signal from the television camera and first control signals at a multiplexing period which is one seventh (1/7) of a clock signal to convert the image signal and first control signals into a first serial signal, a first differential signal circuit for producing first differential signals of the first serial signal, and a second differential signal circuit for producing second differential signals of the clock signal.

Still further, according to the present invention the second connection circuit includes a first differential signal receiver circuit for reproducing the first serial signal from the first differential signals, a second differential signal receiver circuit for reproducing the clock signal from the second differential signals, a first time division de-multiplexing circuit for time division de-multiplexing the time division multiplexed first serial signal, reproduced from the first differential signals by the first differential signal receiver circuit, into the image signal and the first control signals based on the clock signal reproduced from the second differential signals by the second differential signal receiver circuit, and a third differential signal circuit for producing third differential signals from a second control signal.

Still further yet, according to the present invention the transmission cable has a first pair of signal lines transmitting the first differential signals produced from the first serial signal, a second pair of signal lines for transmitting the second differential signals produced from the clock signal, and a third pair of signal lines for transmitting the third differential signals produced from the second control signal from the video apparatus to the television camera.

The above described features of the present invention as now more clearly recited in the claims are not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention as now more clearly recited in the claims are not taught or suggested by Myers, Murata, Monroe, Ueno or Tonkin whether said references are taken individually or in combination with each other as suggested by the Examiner.

Myers teaches a bi-directional high speed video data transmission system, as illustrated in Fig. 1 thereof, having a transmitter and a receiver 140. As per Myers the transmitter 100 receives a parallel video data stream 101-103, a clock signal PCLK and a control signal CNTL. The control signal CNTL and the parallel video data stream 101-103 are encoded as a serial video data stream 110, 120 & 130 and transmitted across a data pair to a receiver, along with the clock signal 150. Myers teaches that this transmission is accomplished by using a pair of transistors 202 & 204, as illustrated in Fig. 2 thereof, to switch a DC current across the two data lines 206 & 208 comprising the data pair. This switching creates an AC current on each data line. Further, as the current varies on the data lines so too does the voltage.

Thus, in Myers the serial video data stream may be transmitted as short bursts of voltage differential measured across a pair of terminating resistors located within the receiver. The clock signal indicates when current is switched from one line to another.

Myers teaches in Fig. 7 thereof a switching diagram for a clock signal CLOCK, and DATA1, and DATA2 signals which are transmitted across data lines 206 & 208 as described above. In Myers the clock signal CLOCK times all transmissions between the transmitter and receiver as described above. The clock signal CLOCK as per Myers switches every n milliseconds from a zero voltage to voltage Vref, and back again at the end of the same time interval. As taught by Myers in Fig. 3 thereof the DATA1 signal represents the video data transmitted by the first bi-directional TMDS circuit 300 which includes a transmitter 100 and a receiver 140, while DATA2 is the signal transmitted by the second bi-directional TMDS circuit 310 which includes a transmitter 100' and a receiver 140' .

As can be seen in Fig. 7 of Myers, the rising edge 702 of the clock signal CLOCK triggers the beginning of a data transmission in DATA1. The DATA1 data transmission similarly ends when the next rising edge 702 of the clock signal CLOCK is reached. In this manner as per Myers, DATA1 may be said to "clock on the rising edge" of the clock signal CLOCK. Similarly, DATA2 clocks on the falling edge 704 of the clock signal CLOCK.

However, as is clear from the above Myers does not teach or suggest that the transmitter 100 includes a first time-division multiplexing circuit for time division multiplexing an image signal from the television camera and first control signals at a multiplexing period which is one seventh (1/7) of a clock

signal to convert the image signal and first control signals into a first serial signal. These features of the present invention are illustrated, for example, in Fig. 2 of the present application and discussed in corresponding sections of the present application, for example, on page 18, lines 13-21. As can be seen in Fig. 2 of the present application there are seven (7) slots (time divided portions) into which the video data and the first control signal are multiplexed across one (1) period T of the clock signal. As per Fig. 2 of the present application the image signal from the television camera and the first control signals are time division multiplexed across one (1) time period of the clock signal to form seven (7) slots of data.

No teaching similar to that described above with respect to the present invention can be found in Myers. In fact Myers teaches as illustrated in Fig. 7 thereof that the DATA1 signal is transmitted across an entire period of the clock signal CLOCK. There is absolutely no teaching or suggestion in Myers that either of the DATA1 or the DATA2 signals are divided and transmitted in seven (7) slots across one (1) period of the clock signal CLOCK as in the present invention as recited in the claims.

Since there is no teaching or suggestion in Myers of time division multiplexed signals as in the present invention, surely there is no teaching or suggestion in Myers of the first differential signal circuit for producing first differential signals of the first serial signal formed by time division multiplexing the video signal and the first control signal, and a second differential signal circuit for producing second differential signals formed by the clock signal as in the present invention as recited in the claims.

Thus, Myers fails to teach or suggest that a first connection circuit includes a first time-division multiplexing circuit for time division multiplexing an image signal from the television camera and first control signals at a multiplexing period which is one seventh (1/7) of a clock signal to convert the image signal and first control signals into a first serial signal, a first differential signal circuit for producing first differential signals of the first serial signal, and a second differential signal circuit for producing second differential signals of the clock signal as recited in the claims.

Still further, Myers fails to teach or suggest that a second connection circuit includes a first differential signal receiver circuit for reproducing the first serial signal from the first differential signals, a second differential signal receiver circuit for reproducing the clock signal from the second differential signals, a first time division de-multiplexing circuit for time division de-multiplexing the time division multiplexed first serial signal, reproduced from the first differential signals by the first differential signal receiver circuit, into the image signal and the first control signals based on the clock signal reproduced from the second differential signals by the second differential signal receiver circuit, and a third differential signal circuit for producing third differential signals from a second control signal as recited in the claims.

The above described deficiencies of Myers are not supplied by any of the other references of record. Particularly, the above described deficiencies of Myers are not supplied by Murata, Monroe, Ueno or Tonkin.

Murata is merely relied upon by the Examiner for an alleged teaching of a time division multiplexing circuit. However, there is no teaching or suggestion in Murata that the transmitter 150 includes a first time-division

multiplexing circuit for time division multiplexing an image signal from the television camera and first control signals at a multiplexing period which is one seventh (1/7) of a clock signal to convert the image signal and first control signals into a first serial signal as in the present invention as recited in the claims. Attention is directed to Figs. 4A-E and 5A-D of Murata that illustrate various timing charts. At no point is there any teaching or suggestion in Murata by way of Figs. 4A-E and 5A-D or the corresponding portions of the specification thereof of the features of the present invention as illustrated in Fig. 2 of the present application wherein seven (7) slots (time divided portions) are formed into which the video data and the first control signal are multiplexed across one (1) period T of the clock signal.

Monroe is merely relied upon by the Examiner for an alleged teaching of providing a control signal which includes an IP signal.

Ueno is merely relied upon by the Examiner for an alleged teaching of producing a control and trigger signals to control a camera remotely.

Tonkin is merely relied upon by the Examiner for an alleged teaching of a line for supplying power from the video apparatus to the camera.

However, the teachings of Monroe, Ueno and Tonkin as per the above do not supply the above noted deficiencies of Myers and Murata. Particularly, Monroe, Ueno and Tonkin do not teach or suggest a first time-division multiplexing circuit for time division multiplexing an image signal from the television camera and first control signals at a multiplexing period which is one seventh (1/7) of a clock signal to convert the image signal and first control signals into a first serial signal as in the present invention as recited in the claims.

Therefore, since each of Myers, Murata, Monroe, Ueno and Tonkin fails to teach or suggest the features of the present invention as now more clearly recited in the claims, combining Myers and Murata with one or more of Monroe, Ueno and Tonkin would not render obvious the claimed invention. Accordingly, reconsideration and withdrawal of the 35 USC §103(a) rejection of claims 1-3, 9, 10, 12, 15-18 and 25-27 as being unpatentable over Myers in view of Murata; the 35 USC §103(a) rejection of claims 4, 19 and 28 as being unpatentable over Myers, in view of Murata and further in view of Monroe; the 35 USC §103(a) rejection of claims 5, 13, 14, 20, 21, 29 and 30 as being unpatentable over Myers, in view of Murata and further in view of Ueno; the 35 USC §103(a) rejection of claims 6, 22 and 31 stand rejected under 35 USC §103(a) as being unpatentable over Myers, Murata in view of Ueno and further in view of Monroe; and the 35 USC §103(a) rejection of claim 11 as being unpatentable over Myers, Murata and further in view of Tonkin are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-33.

In view of the foregoing amendments and remarks, Applicants submit that claims 1, 2, 4-6, 9-11, 13-17, 19-22, 25, 26 and 28-31 are in condition for allowance. Accordingly, early allowance of the present application based on claims 1, 2, 4-6, 9-11, 13-17, 19-22, 25, 26 and 28-31 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (500.43678X00).

Respectfully submitted,

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